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DESIGN OF PHASE LOCKED LOOP

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ABSTRACT

In this work, we have designed CDR-PLL for 1GHz frequency. The design is carried out in the 180nm CMOS technology. We have use Hogge phase detector with the Kim-Lee delay cell based VCO. The designed CDR-PLL is tested by applying the 8B-10B encoded data and the simulation results are represented. The obtained results show that the clock is recovered successfully.

KEYWORDS: CMOS, CDR, PLL, VCO, Phase detector, 8B-10B, Delay-cell

INTRODUCTION

The Phase Locked Loop (PLL) is very versatile circuit and can be found in variety of applications such as microprocessors, disk-drive electronics and serial communication circuits. The PLLs are used to generate on-chip clock, in Clock Data Recovery (CDR) systems as well as for frequency multiplications [1].

In many communication systems, the clock is not transmitted along with data, but it is recovered from the data itself and the recovered clock is used to sample the data. In order to reduce the error, generated clock should have minimum jitter.

In this work, we have implemented CDR PLL to recover clock from 1Gbps data. The generated clock has the frequency 1GHz. The design is carried out using 180nm CMOS technology. The simulation results and physical design of the CDR-PLL is also presented. In Section II, basics of PLL with the block are discussed. The phase detector and its implementation is discussed in Section III. Section IV represents the implementation and simulation of VCO. In section V, overall performance of CDR-PLL is discussed and finally, the conclusions are drawn in section VI.

Basics of PLL

The basic block diagram of the PLL is shown in Figure 1. The PLL contains phase detector, voltage controlled oscillator, loop filter and frequency divider.

The phase detector detects the phase difference between the input reference clock and feedback VCO clock provided by frequency divider. The average output of the linear phase detector is proportional to the phase difference between two input clocks. The phase detector is a digital circuit. The output of the phase detector is passed through the loop filter, in order to get average value of it. The output of the loop filter is fed to the VCO, which generated the output clock. This VCO generated clock is fed back to the phase detector through the frequency divider network.

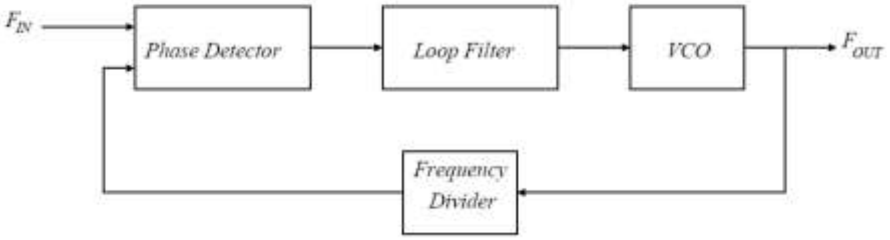

Fig 1 : Basic Block diagram of PLL

The phase detector detects the phase difference between the input reference signal and fed back VCO signal. The output of the ideal phase detector is proportional to the phase error (Φ_{error}). The phase detector is implemented with the help of the Hogge phase detector circuit and charge pump.

Basics of PLL

In Figure 2, the synchronous edge detector[2] is shown. The signal at point B is resulting from the sampling of the data by CLK. Signal at point Y can be obtained by making XOR operation between the signal at B and input data Din. The width of the pulses at Y represents the phase difference between the CLK and Din. The width of the pulses at point Y varies linearly depending upon the phase difference of the CLK and Din. This circuit also produces the pulses for each data transition. This suggests that the synchronous phase detector can be used as the linear phase detector. However, the average voltage output of the synchronous edge detector depends on the data density, failing to produce unique average output voltage depending upon the phase difference for various data pattern. The average output of the synchronous phase detector remains unchanged if the density of the data falls by factor of two and the phase difference raised by same factor, resulting the false locking. To overcome this ambiguity, the proportional pulses at point Y must be accomplished by the reference pulses[3]. The combination of these two pulses eliminates the ambiguity of the data pulses. The reference pulses can be generated by sampling the signal at point B on the negative edge of the CLK and XORed it with signal at B. This is done by the Hogge Phase Detector[4], which is illustrated in the Figure 3.

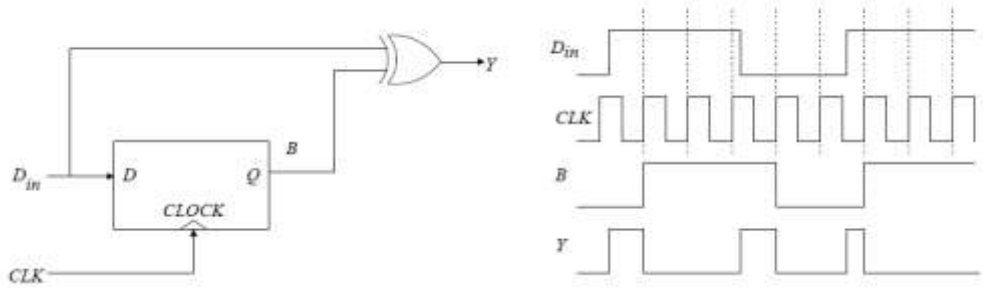

Fig 2 : Synchronous edge detector and its waveform

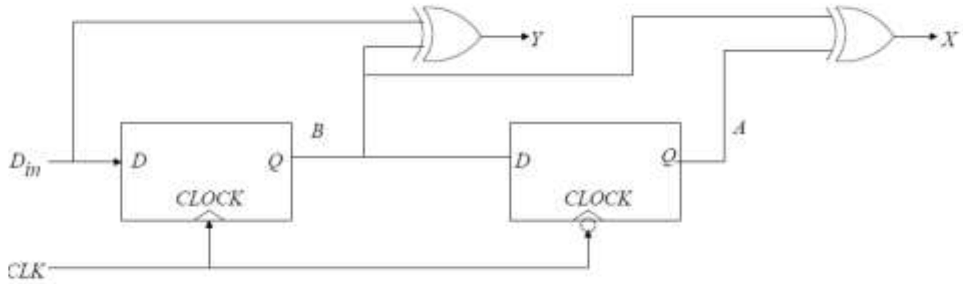

Fig 3 : Hogge Phase Detector

In Hogge phase detector, D-flipflops are used which have the finite delay in signal path. The signal is delayed by ΔT in D-FF. This leads to the width of the pulse at point Y wider than the pulse at the point X by ΔT even thought there is no phase difference at the input. This delay DT can be a significant value in high speed circuit. Such problem can be solved by either making pulse at Y shorter or pulse at X larger by ΔT. The Figure 4 shows the Hogge phase detector in which pulse at Y is made shorter.

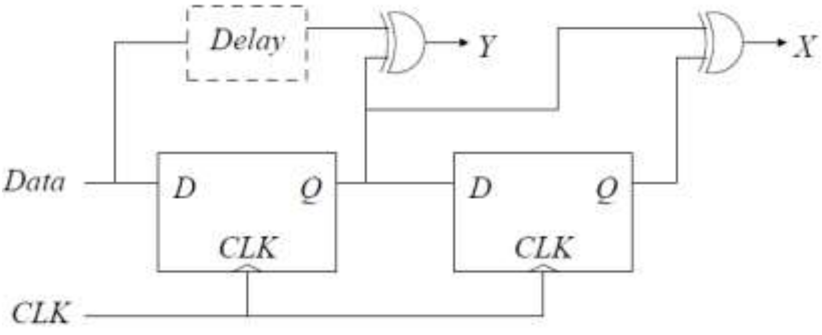

Fig 4 : Hogge Phase Detector with delay

The Hogge Phase Detector consists of two edge triggered DFFs, two EXOR gates and a delay. The circuit of the edge trigger flipflop is illustrated is Figure 5. The delay is realized by the inverter chain. Since DFF contains four inverters and two transmission gates in signal path, six inverters are connected in series to generate almost same delay as introduced by D-FF. The EXOR gates are realized using the NAND gates and inverters. The simulation of implemented Hogge phase detector is shown in Figure 7. While implementing the design, the sizes of PMOS transistors are kept double than that of NMOS transistor. This is necessary to have symmetric logic levels. The two outputs of the Hogge phase detector are combined into single output using the charge pump. The charge pump produces the current pulses according to the output of the Hogge phase detector to drive the loop filter.

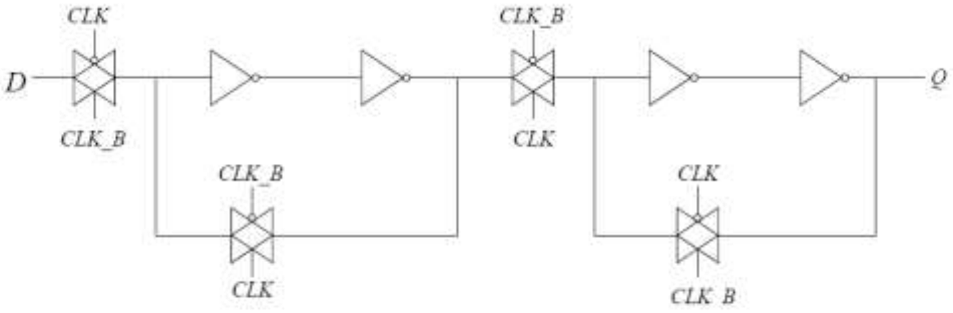

Fig 5 : Edge triggered D-Flip Flop

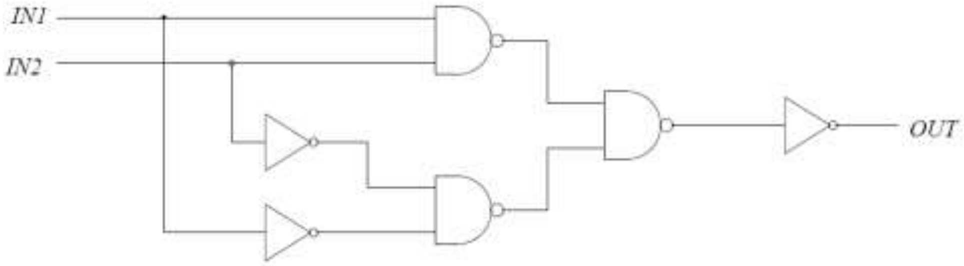

Fig 6 : Ex-or Gate

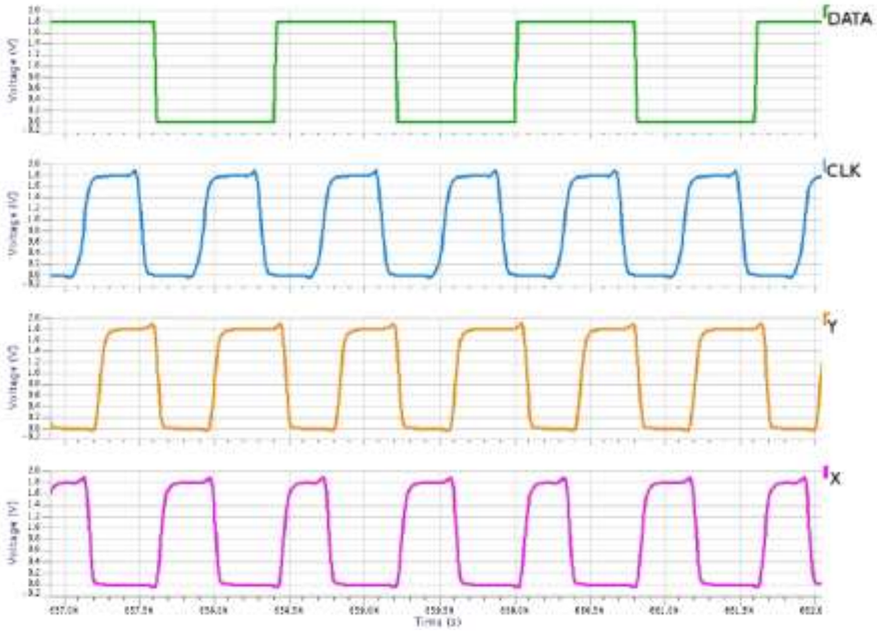

Fig 7 : Simulation result of the Hogge phase detector with delay

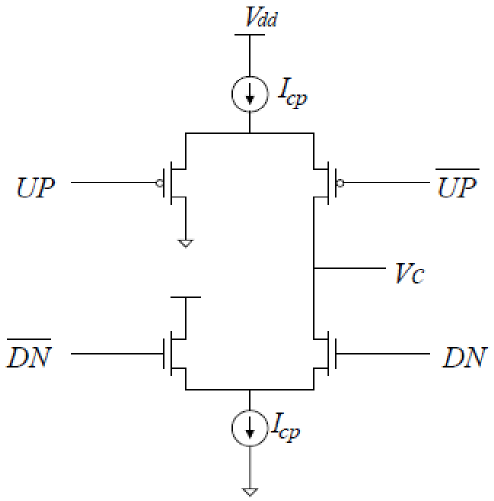

Fig 8 : Simulation result of the Hogge phase detector with delay

The conceptual block diagram of the charge pump is shown in Figure 8. When DN signal is activated, the collected at node Vc is reduced at constant rate. When UP signal is activated the charge at node Vc is accumulated at constant rate. Signal X from the Hogge phase detector is connected to UP signal of charge pump and signal Y is connected to the DN signal of the charge pump. The detail implementation of charge pump is illustrated in Figure 9.

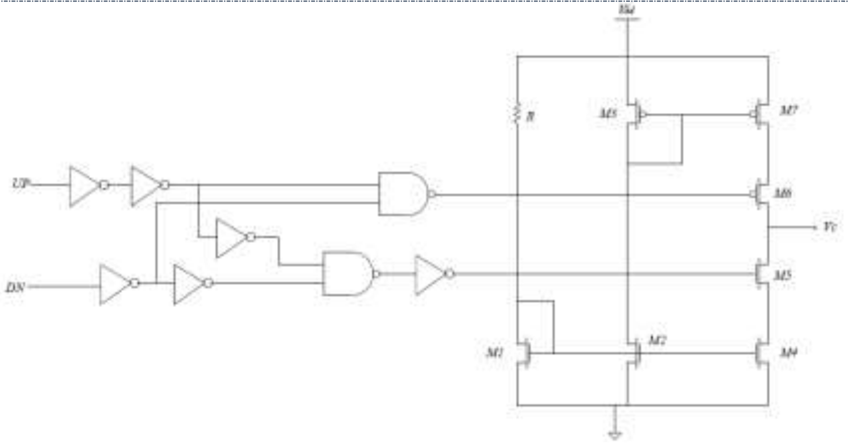

Fig 9 : Implantation details of charge pump

Voltage Controlled Oscillator

The voltage controlled oscillator produces output frequency which is function of the input voltage. The VCO is a key factor in the performance the PLL. In CMOS technology, LC and Ring based VCO are used. Each topology has its advantage and disadvantages. The comparison of the PLL with LC VCO and Ring VCO is presented in [5]. The Ring VCO can be implemented easily, it has wide tuning range and also generate to multi-phase clock, however the noise performance is not as good as LC VCO and the gain is high. LC VCO has better noise performance but suffers from narrow tuning range and it has a complicated design. In this implementation we have used Lee-Kim delay cell based VCO. The other possible implementation of Ring based VCO are discussed in [6] and [7]. The implementation of Lee-Kim Delay Cell based VCO [8] is shown in Figure 10.

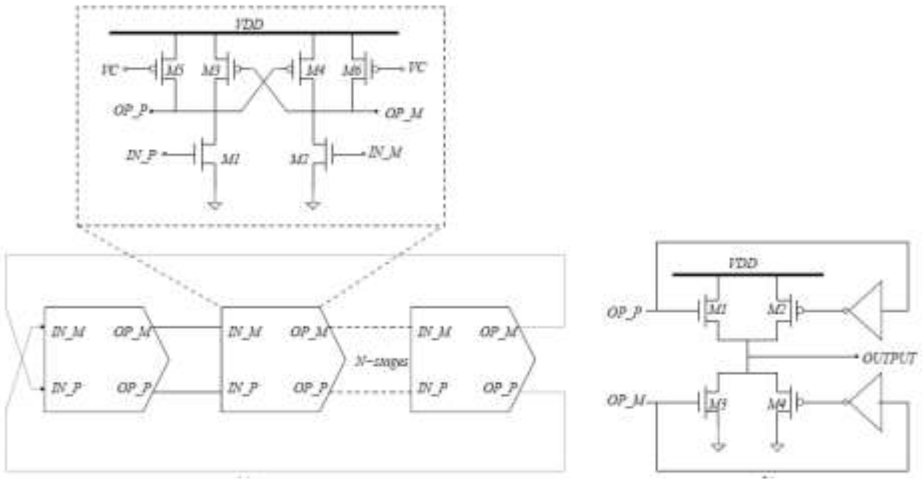

Fig 10 : Implantation details of Lee-Kim Delay Cell based VCO

The simulation of the Lee-Kim Delay Cell based VCO for 1GHz as a lock frequency is shown in Figure 11. The transfer characteristic of the VCO is almost linear over a certain voltage range. Moreover the output of the VCO has 50% duty cycle. This VCO does not require any extra biasing circuit and the frequency range can be changed easily by changing the size of the transistors. The power supply rejection ratio is also better than current starved vco[7] and Maneatis delay cell based VCO[8].

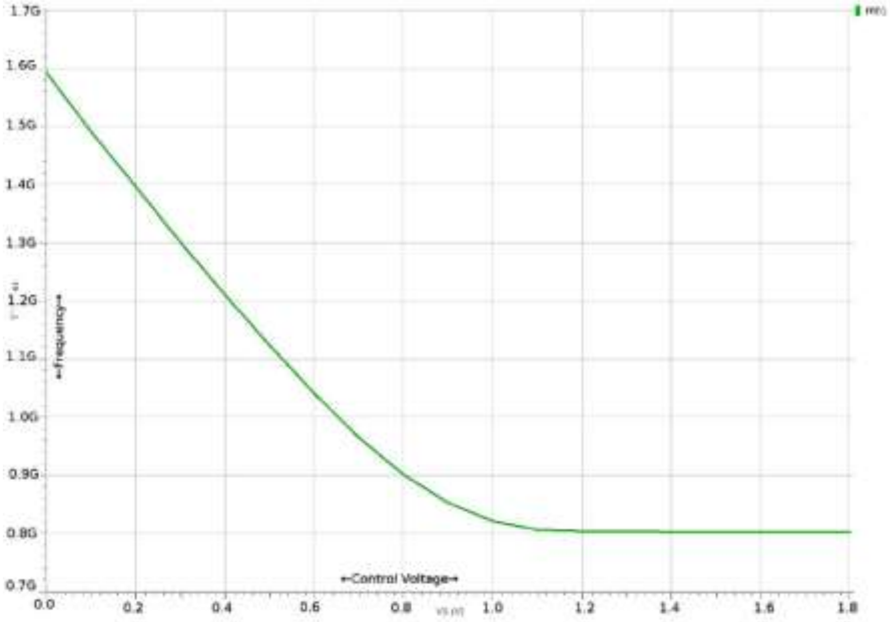

Fig 11 : Simulation result of VCO with Lee-Kim Delay Cell

Clock Data Recovery Phase Locked Loop

Figure 12 represents the complete block diagram of the CDR-PLL. Here we did not use the frequency divider network. As loop filter the second order low pass filter is used.

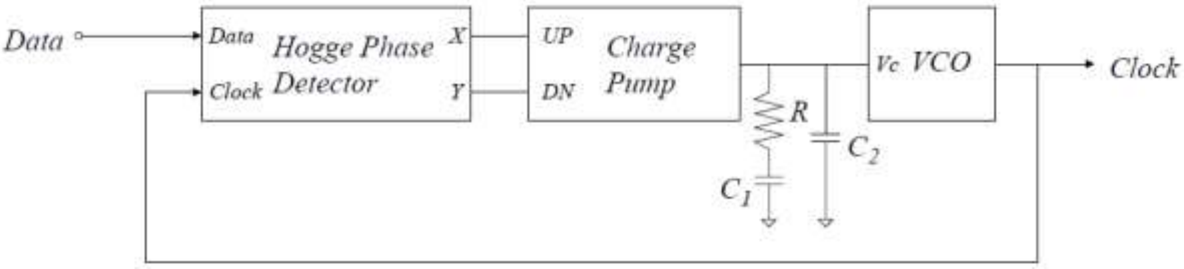

Fig 12 : Block diagram of CDR-PLL

The CDR PLL is designed to support following specifications

- Input data rate : 1Gbits/s
- Input data encoding : 8B-10B
- Length of training sequence : 1us
- Unity gain bandwidth : 20MHz
- Phase Margin : 65 degree

In order to meet mentioned specifications, various components of the CDR-PLL are designed. The specifications of the designed VCO are as follows,

- Center frequency of oscillation : 1.0GHz
- Maximum output frequency : 1.75GHz
- Minimum output frequency : 575GHz
- The gain of VCO : 1.13GHz/V with negative slop

In order to meet the stability requirements, the value of the C1 is fixed to 40pF, C2 is chosen to 2pF and R is set to 0.9KΩ. The charge pump current source value is 124µA. Figure 13 shows the simulation result of the CDR-

PLL, when there is no jitter in input. Figure 14 illustrates the simulation when jitter of 40pS is added into the data sequence. In both cases the PLL remains locked during the data sequence.

In first simulation case i.e. no jitter in input, the maximum output frequency during the data sequence observed is 1.011GHz and minimum frequency observed is 986.6GHz.

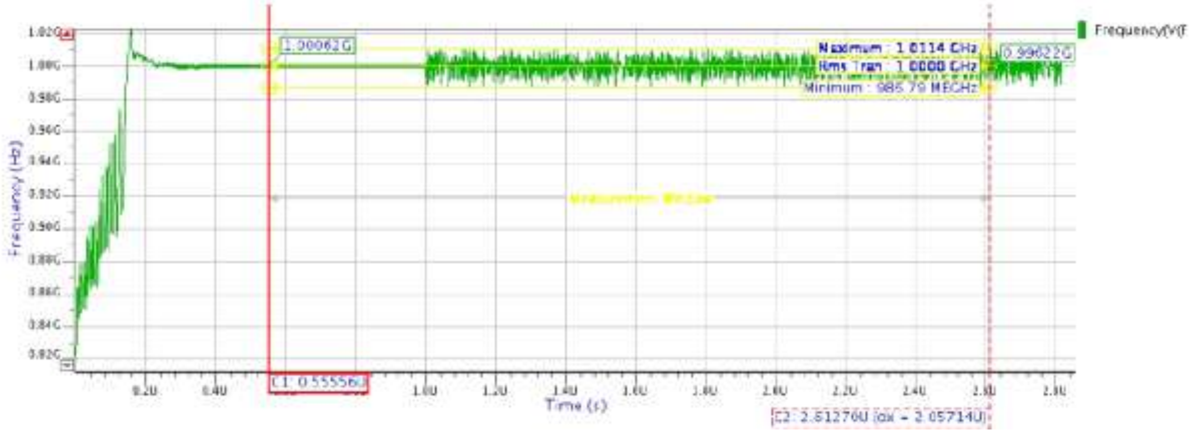

Fig 13 : Simulation result of CDR-PLL with no jitter in input

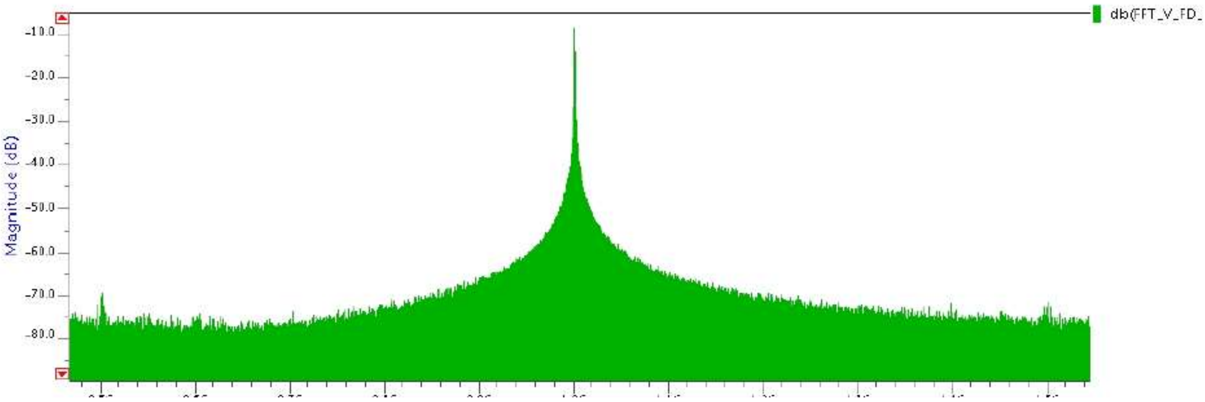

Fig 14 : Spectrum of output when no jitter in input

In second simulation case, 10ps jitter is added to training sequence and 40ps jitter is added to data sequence. The simulation result is displayed if figure 15 and 16. The maximum frequency of output is observed 1.02GHz and minimum frequency is 979MHz.

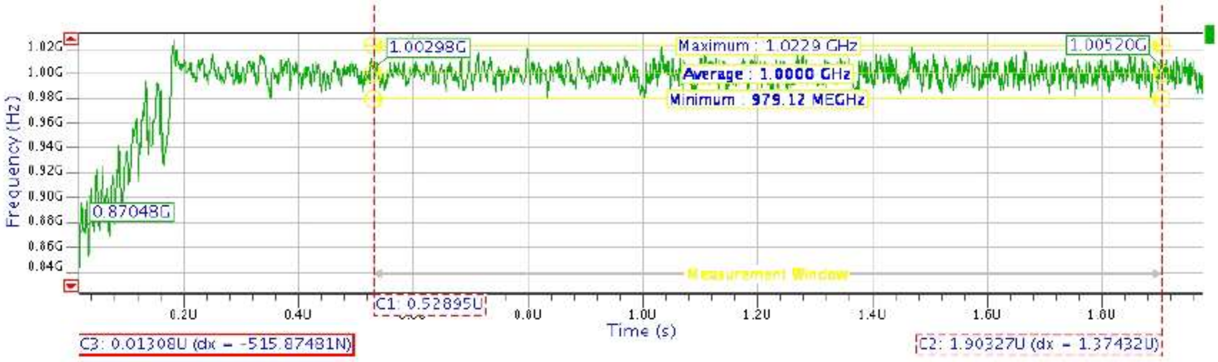

Fig 15 : Simulation result of CDR-PLL with jitter in input

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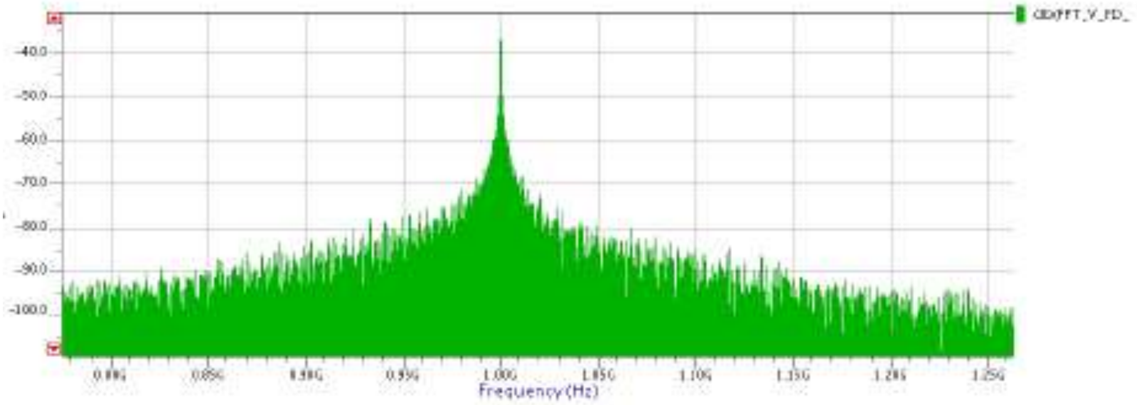

Fig 16 : Spectrum of output with jitter in input

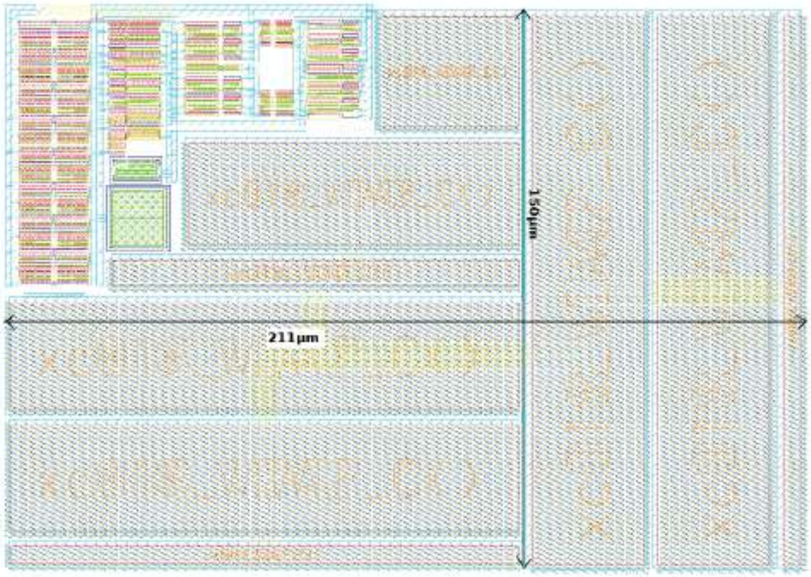

Fig 17 : Physical design of the CDR-PLL

CONCLUSION

In this work we have demonstrated the complete design of the CDR-PLL. The design is to support the data rate of the 1Gbits/second. The design is simulated with jitter in input. During the simulation 8b-10b encoded data sequence is used. Even when the jitter is present in input, the output of the CDR-PLL remains locked.

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